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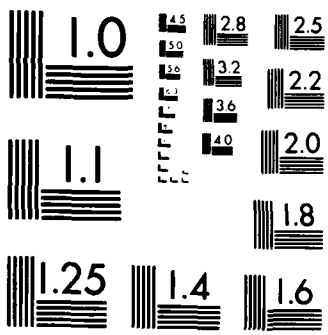

Molecular-Beam Epitaxial Growth and Device Potential of Polar/Nonpolar Semiconductor Heterostructures

Final Report

by

Herbert Kroemer

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20. ABSTRACT

Techniques for the molecular beam epitaxial growth of GaP and GaAs substrates were developed. The techniques rely on the total in-situ removal of all oxygen from the Si surface, to create an atomically clean Si starting surface, coupled with the use of the unusual and previously not used crystallographic (211) orientation for the Si substrate. In the case of GaP growth a third essential ingredient was the use of pure P_2 vapor, generated by the high-temperature decomposition of GaP, rather than the P_4 vapor generated by the evaporation of elemental phosphorus.

Atomic Si surface cleanliness was found essential to good epitaxial growth; it was achieved by developing a new technique for the in-situ removal of SiO_2 through reduction with a Ga vapor beam at 800°C.

The central problem of obtaining device-quality growth of both GaAs and GaP was found to be the problem of avoiding antiphase domains (APDs) in the growing film, that is, of random domains containing opposite assignments of the lattice positions to the Ga and P atoms. On the commonly used crystallographic (100) orientation, APDs are fundamentally unavoidable. The (211) orientation was recognized to have a bond configuration at the interface such that APDs should not form. Experimental (211) growths yielded layers of high quality that were demonstrably free of APDs, as predicted. The recognition of the (211) orientation as the "canonical orientation" for the growth of polar compound semiconductors on non-polar elemental semiconductor substrates was a completely unexpected result of this research, and perhaps the most far-reaching one.

A GaP-on-Si transistor was achieved, vastly better than any previous or concurrent effort towards this goal, but still not with properties sufficiently good to make it a practical competitor to either straight-Si transistors or to all-III/V-compound heterostructure bipolar transistors. GaP-on-Si transistors with properties better than straight-Si transistors could probably be achieved with persistent effort. But the technology to do so would be more complicated than that of all-III/V-compound heterostructure bipolar transistors, which should have even better properties.

Lattice-mismatched (4%) growth of GaAs on Si was achieved, using the clean Si surface technology and the (211) orientation. Although the interface itself in such a mismatched system can never be a low-defect interface, the bulk of the GaAs layers grown on Si appeared to be of device quality. Initial growth results showed a mediocre morphology, but the latter improved drastically when a 100nm-thick GaAs/(Al,Ga)As superlattice buffer layer was first grown directly on the Si substrate.

Because of what appears to be a near-complete suppression of "substrate memory" by the superlattice buffer layer, we believe that GaAs growth on Si is achievable that is of the same quality as that of GaAs on itself, a very significant conclusion.

REPORT ON THE RESEARCH

A. The Problem.

Taken in its broadest "strategic" sense, the objective of this research was to explore some of the limits of the emerging new technology of molecular beam epitaxy, more specifically, to determine to what extent it might be possible by this new technology to grow III/V compound semiconductors such as GaAs or GaP on elemental semiconductor substrates such as Si or Ge, preferably the former. At the time this research was initiated, a number of such attempts using other technologies had already been undertaken, all without exceptions ending in dismal failures. A variety of preliminary considerations suggested that MBE might have a chance.

Initially, it was expected that a close lattice match between the compound semiconductor and the Si substrate would be necessary not only for a low-defect interface but for acceptable growth quality itself. This naturally led to the reasonably well lattice matched pair GaP-on-Si (mismatch 0.4%), at least for the initial work, with GaAs-on-Ge as a backup in the (not unlikely) event that GaP-on-Si might prove untenable.

Within this general framework, a more specific objective was the achievement of a heterostructure bipolar transistor (HBT) [1] in which a GaP emitter was grown on top of a base/collector structure made of Si. If successful, such a transistor was predicted to have an appreciably higher speed -- we estimated a factor 2.8 -- and hence would be of great practical interest. However, it was recognized by both us and ARO that this was a high-risk project, and the GaP-on-Si HBT was at least as much a *vehicle* for pushing MBE technology itself to its limits, as it was a research objective in its own right.

At a later stage in the work, after our own research showed that lattice-matching was essential only for the quality of the interface, but not for that of the subsequent epitaxial growth itself, we returned to the broader objective stated in the opening paragraph, and set ourselves the specific objective of determining whether or not device-quality GaAs could be grown on Si substrates.

A-1

B. Summary of Results.

a) The SiO_2 Problem.

It had been recognized from the outset that, in order to achieve both the long-term "strategic" goal and the more tangible short-term transistor goal, a number of problems would have to be overcome. One of the problems whose seriousness had been specifically recognized, was the need to somehow create a Si surface completely free of SiO_2. This problem had been the principal source of difficulties for others, and its tractability was by no means certain. The problem was solved early during the research effort, by developing a new technique [2] for the in-situ removal of SiO_2 through reduction with a Ga vapor beam at 800°C. This was an important contribution to MBE technology as a whole, going significantly beyond the specific research problem at hand.

b) The Phosphorus Problem.

A second problem the existence of which had also been recognized from the outset, and from which severe difficulties had been expected, concerned the need to handle phosphorus in an MBE system. This problem, too, was solved early during the research effort: We found that the vacuum problems others had encountered, who had used a source of *elemental* phosphorus, could be reduced by several orders of magnitude, by using instead the thermal decomposition of GaP to generate the phosphorus vapor beam [3]. Such a source generates a beam of P_2 molecules, which cause only relatively minor vacuum difficulties, as opposed to the P_4 molecules generated from elemental phosphorus.

c) The Antiphase Domain Disorder Problem.

A third problem the existence of which had been recognized from the outset -- but not its severity -- was the problem of avoiding antiphase domains (APDs) in the growing GaP film, that is, of random domains containing opposite assignments of the lattice positions to the Ga and P atoms. We were -- and are -- convinced that any III/V compound semiconductor film containing APDs would be useless for true device-quality material. It had also been clear that on the crystallographic (100) orientation APDs were fundamentally unavoidable, due to the presence of unavoidable atomic-height steps, which nucleate APDs. But the solution of this problem had been expected to be simple: a change in growth orientation to the (111) orientation, rarely used in MBE growth, but known not to form APDs even in the presence of steps, and not expected to present any serious growth difficulties. The latter turned out to be an illusion: As a result of a previously not recognized electrostatic charge imbalance at the (111) interface between a polar compound semiconductor and a non-polar elemental semiconductor [4], such an interface would behave as if it were extremely heavily n-type doped, and in addition, it would have a very high concentration of structural defects. In fact, only a very small minority of orientations are free of this imbalance, namely those for which the interface plane is parallel to one of the four tetrahedral <111> bond directions. The simplest of these is the (110) plane. Some experiments in which we had used (110) substrates accidentally, and which had yielded an excellent visual morphology, misled us for several months into believing that the reconstruction thought to be naturally present on this orientation would prevent the other problem, APD formation, from occurring [5]. This, too, proved to be an illusion, and for a while it appeared that the solutions to the APD problem and to the charge imbalance problem were mutually exclusive. We were about to give up, when we recognized theoretically [6] that the obscure and previously never used (211) orientation, which was one of the orientations for charge-free interfaces, had a bond configuration at that interface

such that APDs would probably not form. Experimental (211) growths quickly yielded layers of surprisingly high quality, which were demonstrably free of APDs [6],[7].

d) Emergence of the (211) Growth Orientation.

The recognition of the (211) orientation as the "canonical orientation" for the growth of polar compound semiconductors on non-polar elemental semiconductor substrates was a completely unexpected result of this research, and perhaps the most far-reaching one. Ultimately, it drastically changed the character of the research, from a project that was basically device-oriented with only an incidental material science component, to a project that was predominantly materials science-oriented , with the transistor serving more as a particularly sensitive diagnostic indicator of the materials and interface quality, than as a principal goal in its own right.

e) GaP-on-Si Transistor

A GaP-on-Si transistor was achieved [7], vastly better than any previous or concurrent effort towards this goal, but still not with properties sufficiently good to make it a practical competitor to either straight-Si transistors or to all-III/V-compound HBTs. Although the quality of the GaP layers was surprisingly good, the hetero-interface itself contained enough residual defects to make the transistors marginal. This was not surprising: Even in the much easier MBE growth of GaAs and (Al,Ga)As on GaAs, the substrate-to-epilayer growth start interface is *always* avoided as a critical interface inside the device itself, especially in a minority carrier device. Against this background, our achievement of transistors with such an interface was actually quite remarkable. Our research suggested that GaP-on-Si transistors with properties better than straight-Si transistors could probably be achieved with persistent effort. But it was clear that the technology to do so would be more complicated than that of all-III/V-compound HBTs, which should have even better properties. Under these circumstances, there appeared little incentive to pursue the goal of a GaP-on-Si transistor beyond what had been achieved, and we turned to the exploitation of the numerous conceptual and technological developments that had accumulated during the research.

e) Defects in GaP-on-Si(211) Layers.

With the help of others, extensive defect studies on the quality of the GaP-on-Si layers were conducted, mainly by transmission electron microscopy (TEM). These studies, which remain to be published, showed that the layers were completely free of APDs, and had a surprisingly low dislocation density, much lower than one would have expected from the number of misfit dislocations necessary to accommodate the non-negligible lattice mismatch (0.4%) between GaP and Si. Evidently, only few of the misfit dislocations propagate upwards into the bulk of the epitaxial layer! The dominant defects appeared to be stacking faults, the electrical consequences of which are unknown.

f) GaAs-on-Si(211) Growth.

Encouraged by the surprisingly good results with GaP-on-Si growth, and by successful ONR-sponsored work of ours on the growth of (Al,Ga)Sb superlattices on badly mismatched (>7%) GaAs substrates [8], we turned in early-1984 towards the mismatched (4%) growth of GaAs on Si, using the clean Si surface technology and the (211) orientation that were so successful with GaP-on-Si. Although the interface itself in such a mismatched system can never be a low-defect interface, it would be of very large practical interest, especially for integrated optoelectronics, if the remainder of GaAs layers grown on Si could be made of device quality. Initial growth results showed a mediocre morphology

[9], but the latter improved drastically when a 100nm-thick GaAs/(Al,Ga)As superlattice buffer layer was first grown directly on the Si substrate [10]. Photoluminescence measurements on (211)-oriented GaAs/(Al,Ga)As superlattices over a GaAs/(Al,Ga)As superlattice buffer layer on GaAs rather than Si substrates [11] (under ONR sponsorship) showed the resulting growth to be at least as good as conventional (100) growth. Because of what appears to be a near-complete suppression of "substrate memory" by the superlattice buffer layer, we expect these favorable results to carry over to GaAs-on-Si growth. If this expectation should prove correct, it would mean nothing less but that GaAs growth on Si might be achievable that is of the same quality as that of GaAs on itself! This is where our work stood at the time of the expiration of this contract. It is continued to be pursued under a current follow-up ARO contract.

g) GaAs-on-Ge Growth.

Because of the obvious analogy of the GaAs/Ge system to the GaP/Si system, and because GaAs/Ge appeared initially the simpler of the two systems, a substantial amount of research on the growth of GaAs on Ge was conducted during this contract. We found, quite unexpectedly, that the growth of GaAs on Ge is in fact the far more difficult of the two, largely because of a strong chemical interaction between the arsenic and the Ge substrate, which interfered with the growth [13]. To suppress this interaction, the growths had to be conducted at a temperature below 400°C, far too low to yield GaAs of minimum acceptable quality. By contrast, in the case of GaP-on-Si the reaction between P and Si remains within acceptable bounds below about 580°C, about 30°C above the minimum growth temperature of 550°C for good GaP [7]. Inasmuch as under this contract GaAs-on-Ge was of little interest in its own right, but only of interest in support of the GaP-on-Si work, all GaAs-on-Ge work was eventually transferred to one of our ONR contracts, which called for the study of GaAs/Ge/GaAs double heterostructures. The work remained unsuccessful, and it was eventually dropped altogether. As a result of our experiences with GaAs-on-Ge growth we take a very negative view of claims scattered throughout the literature [12] that the growth of GaAs on Si is facilitated by a germanium interlayer, or that such an interlayer might even be necessary. Our own work flatly disproves the stronger of the two claims, and it speaks strongly against the validity of the weaker claim. We believe that these claims simply reflect their originators' working with Si surfaces that were not completely free from SiO_2 contamination. This leads to poor GaAs growth indeed, which might very well be made less bad by covering up the oxide with Ge. In fact, the originators of the Ge interlayer technique have recently admitted that such an interlayer is not necessary [12].

h) Understanding of Band Lineups.

In the course of our work on both Gap and GaAs on Si we were compelled to conduct a limited amount of work on a few necessary background items. The only item of significance was some work on the continuing problem of band lineups at heterojunctions [14],[15], co-supported by ONR.

C. Publications and Technical Reports

"Reduction of Oxides on Silicon by Heating in a Gallium Molecular Beam at 800°C", S. Wright and H. Kroemer, Appl. Phys. Lett. 35 (#3), pp. 210-211, February 1980.

"On the (110) Orientation as the Preferred Orientation for the MBE Growth of GaAs on Ge, GaP on Si, and Similar Zinc-Blende-on-Diamond Systems", H. Kroemer, K. J. Polasko and S. L. Wright, Appl. Phys. Lett. 36 (#9), pp. 763-765, May 1980.

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"Heterostructure Bipolar Transistors and Integrated Circuits", H. Kroemer, Proc. IEEE, 70 (#1), pp. 13-25, January 1982.

"Operational Aspects of a Gallium Phosphide Source of P_2 Vapor in Molecular Beam Epitaxy", S. L. Wright and H. Kroemer, J. Vac. Sci. Technol. 20 (#2), pp. 143-148, February 1982.

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